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Impact of gate protection silicon nitride film on the sub-quarter micron transistor performances in dynamic random access memory devices

J.H. Choy†

Department of Physics, Simon Fraser University, Canada

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Abstract Gate protection SiN_x as an alternative to a conventional re-oxidation process in Dynamic Random Access Memory devices is investigated. This process can not only protect the gate electrode tungsten against oxidation, but also save the thermal budget due to the re-oxidation. The protection SiNx process is applied to the poly-Si gate, and its device performance is measured and compared with the re-oxidation processed poly-Si gate. The results on the gate dielectric integrity show that etch damage-curing capability of protection SiN_x is comparable to the re-oxidation process. In addition, the hot carrier immunity of the SiN_x deposited gate is superior to that of re-oxidation processed gate.

Key words Dynamic Random Access Memory, Metal-oxide-silicon field-effect transistor, Gate, Breakdown, Hot carrier

1. Introduction

In the modern technologies of the Dynamic Random Access Memory (DRAM) devices, the gate length shrinks to 0.1 μm or less, and raises the problem of the gate resistance-capacitance (RC) time delay that may limit the device performance. In search of a new gate electrode material with low-resistivity, the metal-oxide-silicon field-effect transistors (MOSFETs) with tungsten-based poly-silicon metal gate has been one of the promising candidates to solve RC delay, and has been developed for years. The tungsten (W)/barrier metal/ poly-silicon gate has widely been studied and developed because tungsten has lower resistivity than tungsten silicide, and has good thermal stability and low diffusivity [1-3]. In terms of the device reliability, the re-oxidation of the gate, which grows a thin natural oxide on the substrate and on the gate poly-silicon side wall after gate etch, is one of the major concerns. This process effectively cures the damaged gate dielectric at the gate edge caused by gate etch. Unlike for the conventional polycide (WSi_x) gate, it has been well known that the oxide-growing condition should be well controlled in order to ensure that only (poly)silicon will oxidize and leave tungsten unharmed during the process, which is known as selective re-oxidation [2]. Thermodynamic condition for this process is also well defined. The problems however, still remain on the non-uniformity of the process in terms of the oxide film thickness, and on the process temperature as high as 1,100°C. The re-oxidation typically grows 5~8 nm in thickness, and its effect on the impurity doping profile at the gate edge is known to be quite significant [4]. In addition, efforts are being made to reduce the unnecessary high temperature process as it often creates mechanical strain within the wafer.

As an alternative to the gate re-oxidation, we here introduce the protection SiN_x process, which is composed of only the deposition of CVD SiN_x without high temperature anneal. In this study, the poly-silicon gates are fabricated employing two different processes, protection SiN_x and re-oxidation. Their nMOSFET performance is compared in order to analyze the gate etch damage curing capability of the protection SiN_x process.

2. Experimental

Table 1 summarizes the overall gate process employed in this study. For both protection SiN_x, and re-oxidation processes, N_2O gate dielectric of 40 nm is employed. Then the poly-silicon electrode of 250 nm is deposited. The gate capping layers are nitride and tetra-ethyl-ortho-silicate (TEOS) oxide. Reactive ion etching is used for gate patterning, and is followed by post-etch cleaning. For the gates that applies protection SiN_x process, CVD SiN_x with 8 nm thickness is deposited, while for the gates applying re-oxidation process, 4 nm oxide film is grown on the substrate. After the re-oxidation is done,

†Corresponding author
Tel: +604-291-4082
Fax: +604-291-3592
E-mail: junhoc@sfu.ca

Table 1
Gate process employed for the present study

Cate dielectric (4 nm)	
Gate Poly-Si deposition (250 nm)	
Gate Capping SiN_x/TEOS deposition	
Gate patterning	
Cleaning	
SiN_x dep. (10 nm)	Re-oxidation
NM I/I : As $1.0\times10^{14}/cm^2$	
Spacer TEOS (90 nm)	
NP I/I : As $3.0\times10^{15}/cm^2$, Ph 2.0×10^{13}	

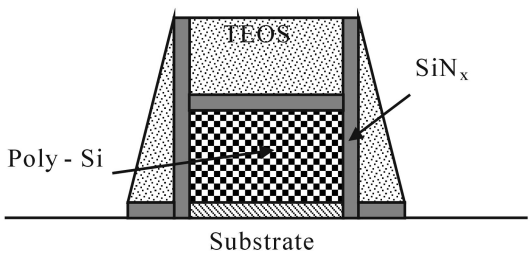

Fig. 1. A schematic gate profile upon completion of the gate protection SiN_x process.

the oxide thickness on the poly-silicon side wall, which is 1.5~2 times larger than that on the substrate is normally observed. Then the gates for both groups are processed to have the normal lightly-doped drain (LDD) structures. Arsenic (As) implantation of dose $1.0\times10^{14}/cm^2$ is applied, and LDD spacer TEOS of length 90nm is formed. The implantation of As and Phosphor were done with 3.0×10^{15} and $2.0\times10^{13}/cm^2$, respectively. In Fig. 1, the schematic gate profile upon completion of the gate protection SiN_x process is displayed.

Using the nMOS capacitors thus processed, the gate dielectric breakdown voltages [5] are made. The capacitor is gate-edge intensive pattern so that the effects of the gate etch damage may be readily monitored. In order to evaluate both the low field dielectric leakage and the dielectric breakdown field, constant gate currents of Ig = 1 μA/cm^2, and 1 A/cm^2 are applied on the capacitors, and the voltage across the gate dielectric, V_g is measured at room temperature. The nMOSFET lifetime against hot carrier stress [6] is also measured to ensure the long-term performance. Using the devices with gate length = 0.18 μm, the drain is stressed at largest substrate current, I_{sub} where the device performance degradation is known to be maximized. By switching the drain and source of the transistor, the drain saturation current I_{ds} is monitored. The lifetime of the device is formally defined as the stress time when I_{ds} decreases to 10% of its initial value.

3. Results and Discussion

Figure 2 shows the cumulative distribution curves of gate dielectric voltages for nMOS capacitors processed by SiN_x and re-oxidation. At low electric field region (1 μA/cm^2), V_g~–3.4 V, and at high field (1 A/cm^2), V_g~ –6.2 V for both cases. The measured data over 15 samples are uniform for both cases, which indicates that the gate etch damage curing capability of SiN_x film at the gate edge is comparable to that of re-oxidation process.

Figure 3 depicts the results of hot carrier injection into nMOSFET of gate length, 0.18 μm. For at least 3 measurements of stress times for each process, the device lifetime may be given by the linear curve as a function of the reciprocal of the drain voltage, $1/V_{ds}$, where the subscript ds refers to a quantity across drain and source

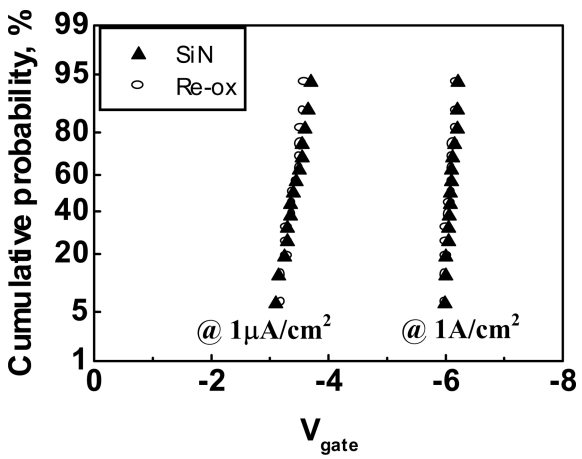

Fig. 2. Cumulative probability showing gate dielectric breakdown voltage distributions of nMOS capacitors employing SiN_x (solid) and re-oxidation (open) processes. For each case, measurements were made at gate current, I_g = 1 μA/cm^2 and 1 A/cm^2.

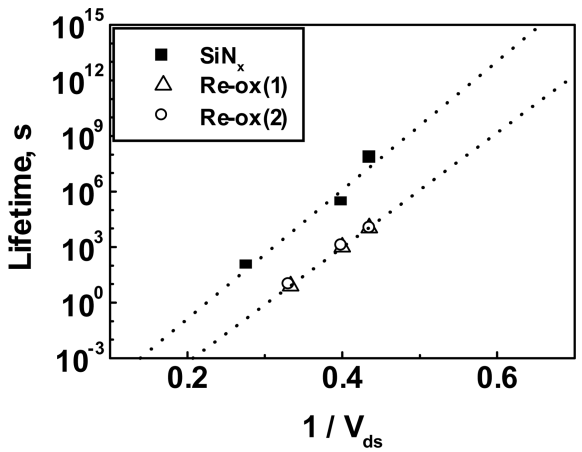

Fig. 3. nMOSFET lifetimes against hot carrier injection. Lifetime for SiN_x deposited gates is higher by 3 orders of magnitude than that with re-oxidation process.

of the transistor. Throughout the entire V_{ds} range, the results show that approximately 3 orders of magnitude longer lifetime is expected for SiN_x deposited devices compared to the devices processed by re-oxidation. It is suspected that such a large performance improvement may come from the difference in electric field at gate edge. The source for such a difference in electric field may be that the protection SiN_x process, compared to re-oxidation, skips the high temperature thermal process, and has slightly larger film thickness on the substrate and on the poly-silicon side wall, thereby resulting in the different doping profile after subsequent implant processes. Concerning the maximum parallel channel electric field, E_m, the following empirical relationship with substrate current, I_{sub} holds,

$$I_{sub} \sim I_{ds} \exp[-1.7\times10^{-6}/E_m] \quad (1)$$

Where E_m is in the unit of V/cm. Figure 4 displays τ^*I_{ds} vs. I_{sub}/I_{ds} relationship for both processes. Each arrow in the figure designates the (τ^*I_{ds}) values measured under an identical stress condition for both devices. However, (τ^*I_{ds}) values of SiN_x deposited devices are still larger than those processed with re-oxidation even when these points are located on the linear curve of re-oxidation processed devices. It indicates that the difference in E_m alone may not explain the improved performance. The slope of the linear curve in Fig. 4, m is, $m = \phi_{it}/\phi_{im}$, where ϕ_{it} and ϕ_{im} are energy require to create an interface state, and impact ionization energy (= 1.24 eV), respectively. According to the results in Fig. 4, ϕ_{it} = 4.5 eV for SiN_x deposited devices, and is higher than that of re-oxidation processed, ϕ_{it} = 3.7 eV. The energy difference shows that the substrate/SiN_x and substrate/re-oxidized interfaces are different each other in quality,

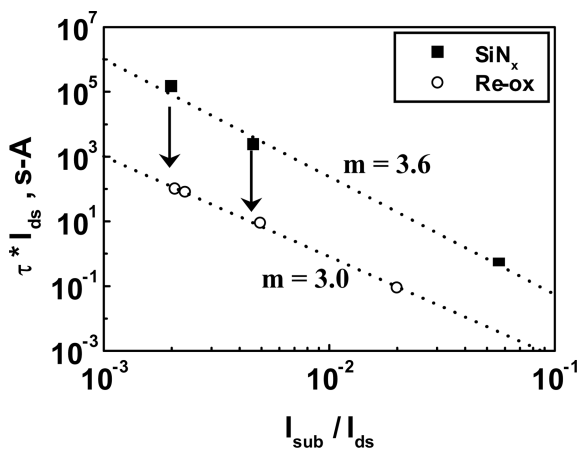

Fig. 4. I_{sub}/I_{ds} dependence of nMOSFET upon hot carrier injection. The slope, m, indicates the energy required to create the interface state, and is higher for SiN_x deposited gates.

and that the former shows improved quality in terms of interface state generation.

4. Summary

We investigate the gate protection SiN_x of thickness 10 nm as an alternative to a conventional re-oxidation process, using the poly-Si gate. The device performance was measured and compared with the re-oxidation processed poly-Si gate. The results on the gate dielectric integrity show that etch damage-curing capability of protection SiN_x is comparable to the re-oxidation process. The hot carrier lifetime of the SiN_x deposited gate is found to improve by 3 orders of magnitude compared to that of re-oxidation processed gate.

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