Journal of the Korean Crystal Growth and Crystal Technology
Vol. 25, No. 1 (2015) 13-19
http://dx.doi.org/10.6111/JKCGCT.2015.25.1.013

p-ISSN 1225-1429
e-ISSN 2234-5078

The relationship between minority carrier life time and structural defects in silicon ingot grown with single seed

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(Received January 21, 2015)
(Revised January 28, 2015)
(Accepted February 6, 2015)

Abstract Among the various possible factors affecting the Minority Carrier Life Time (MCLT) of the mc-Si crystal, dislocations formed during the cooling period after solidification were found to be a major element. It was confirmed that other defects such as grain boundary or twin boundary were not determinative defects affecting the MCLT because most of these defects seemed to be formed during the solidification period. With a measurement of total thickness variation (TTV) and bow of the silicon wafers, it was found that residual stress remaining in the mc-Si crystal might be another major factor affecting the MCLT. Thus, it is expected that better quality of mc-Si can be grown when the cooling process right after solidification is carried out as slow as possible.

Key words Dislocation, Twin boundary, Grain boundary, Minority carrier life time, Residual stress

1. Introduction

These days, more than (60%) of solar cell is produced with multi-crystalline silicon. It is popularly known that single crystalline silicon solar cell is superior to multi-crystalline silicon in cell conversion efficiency. However, single crystalline silicon solar cell has two major drawbacks such as Light Induced Degradation (LID) and high production cost [1-3]. This is the main reason why multi-crystalline silicon is more favored in the solar cell production. Still, multi-crystalline silicon needs to be more improved to have higher cell conversion efficiency in solar cell. Two kinds of problems must be solved to fulfill this target. One of them is inclusions which are introduced during the crystal growth process and the other one is crystal defects like grain boundary, dislocation, twin boundary, and residual strain [4, 5]. It is known that cell efficiency is dominantly affected by the presence of dislocation [6]. This is due to the hosting character of dislocation for the metal impurities, which in turn act as recombination centers for electrical carriers [7]. Dislocations are known to be produced by the stress generated during crystal growth and the related cooling process [8].

Size of grain is dependent on the growth rate of the crystal and presence of seed. Faster cooling will result in smaller grains due to the higher generation rate of crystal nuclei [9-11]. Also, crystal with larger grain or mono-like multi-crystalline silicon crystal can be produced from the seed located at the bottom of the crucible. Regardless of seed, thermal stress is the main source causing defects like dislocation or grain boundary [7].

Further, twin boundary is known to be created during the silicon crystal growth process. This depends on the orientation of the crystal [12]. However, dislocations and twin boundary is generated due to the stress caused by the temperature gradient during the crystal growth and cooling period of ingot. Temperature gradient produces thermal stress which can cause not only so many of the defects mentioned above but also residual stress. This residual stress will cause some amount of strain residing in the silicon wafers after the machining of the silicon ingot. This residual strain will appear as warp, TTV, bow, and saw mark after the slicing of the silicon ingot.

Thus, it would be interesting to see the effect of the growth parameters such as growth speed or cooling speed on the generation of defects mentioned above and their relationship with the MCLT of the silicon crystal. To eliminate the effects of the crucible surface on the generation of grain nucleation, a large single crystalline seed is placed at the bottom of the crucible before the melting of the silicon charge. In the production of the mono-like multi-crystalline silicon ingot, it is well-known to use many seeds of plate shape. However, the

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gap between the plate shape seeds will cause the generation of dislocation during and after the growth of the silicon ingot [13]. In this investigation, just one large seed obtained from the shoulder of Czochralski process was used to avoid the gap effects of the several seeds.

In this way, the relationship between growth parameters and MCLT value will be obtained through defect and residual strain analysis.

2. Experimental Procedures

A large single piece of single crystalline silicon is prepared from the shoulder of the Czochralski grown silicon crystal. This large silicon piece is conical-shaped and is used as the seed for this experiment. This seed is placed at the bottom of the crucible. On top of this seed, 10.8 kg poly-silicon is stacked. To make the silicon ingot have proper resistivity, p-type master alloy containing the boron of 109 ppm was added to this charge. Two silicon ingots of 12 kg were solidified with directional solidification furnace as shown in Fig. 1. The growth parameters employed in this experiment are shown in Fig. 2. As can be seen in Fig. 2, B-ingot was grown and cooled down with lower speed than A-ingot.

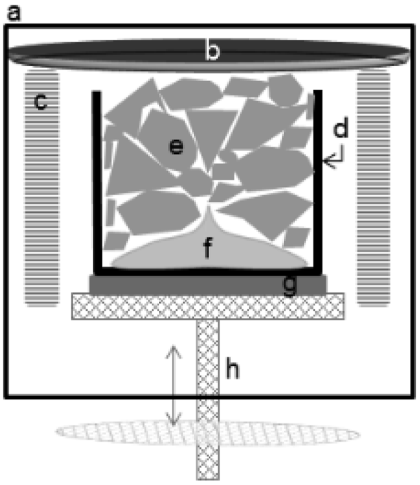

Fig. 1. Furnace for multi-crystalline silicon ingot growth: (a) low vacuum chamber, (b) hard felt insulator, (c) graphite heater, (d) crucible with silicon nitride coating, (e) virgin poly-silicon, (f) single crystal seed, (g) cooling plate, (h) lowering device.

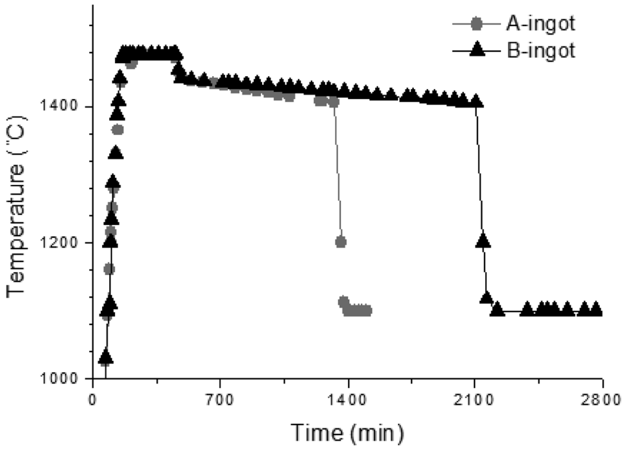

Fig. 2. Silicon crystal growth condition; A-ingot: standard solidification, B-ingot: slower solidification.

After growth, two ingots were cut into several pieces of bricks and sliced into wafers 180 ± 10 μm thickness. Samples were taken from a relevant position from each ingot to measure oxygen and carbon concentrations with FT-IR (NanoMatrix). MCLT was measured with μ-PCD (semi-lab) and TTV, saw mark, warp, and bow of silicon wafers were measured with laser displacement sensor (HANMI Semiconductor). Most silicon wafers were etched preferentially to observe structural defects such as dislocation, grain boundary, and twin boundary with optical microscope.

3. Results and Discussion

3.1. Relationship between MCLT and Structural Defects

The MCLT map of each specimen taken from three parts; i.e., bottom, middle, and top position of each ingot are shown in Fig. 3. As can be seen in this figure, MCLT was generally lower at the edge of the silicon wafers than the central area of wafers. We can expect that this fact might be due to the high density of dislocation generated from the side of the crucible. However, the area of lower MCLT was not in proportion to the defect density only. This might be due to the possibility of residual stress remaining near the edge of the silicon crystal. Changing the crystal growth parameters will change the thermal history of each part of the silicon ingot. The effect of thermal history change on the residual stress will be discussed later in this session.

As can be seen in this figure, the average MCLT near the bottom position of the ingot was higher than the MCLT of the top position of the ingot regardless of the growth speed. There might be two reasons for this phenomenon. One of them is the possibility of the accumulation of the impurities during the growth process. Thus, the concentration of impurities including dopant normally will be higher at the top position of the ingot than the bottom position. These impurities will act as recom-

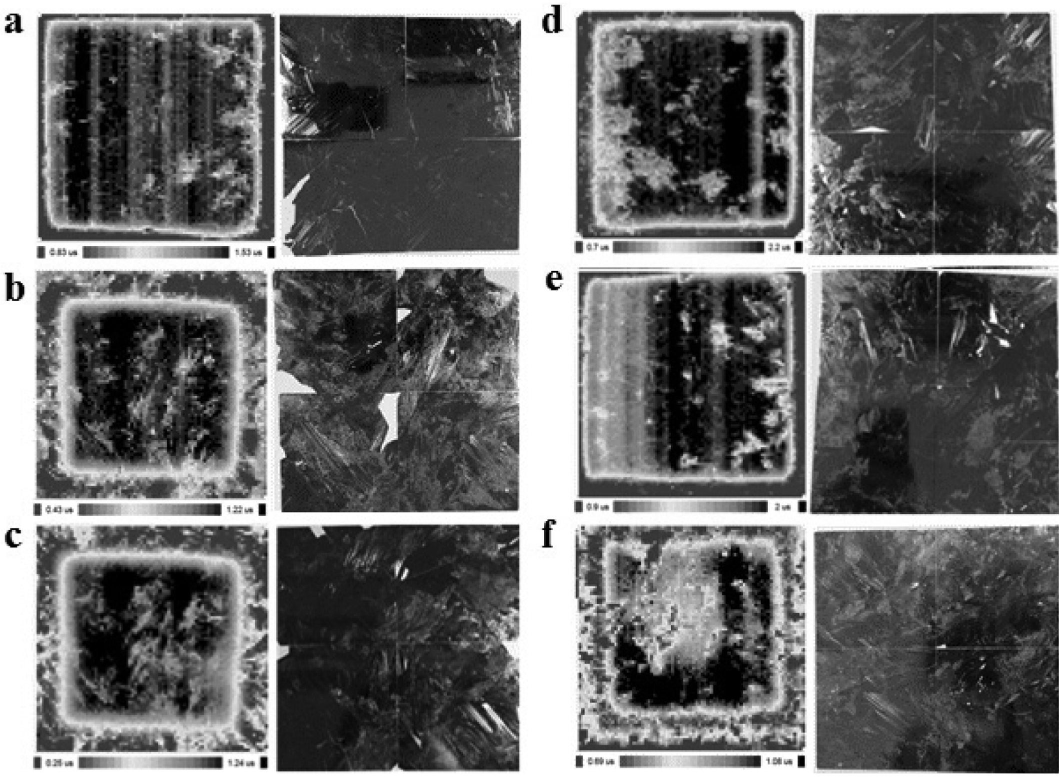

Fig. 3. MCLT map and photograph of wafer surface: (a) bottom position of A-ingot, (b) middle position of A-ingot, (c) top position of A-ingot, (d) bottom position of B-ingot, (e) middle position of B-ingot, (f) top position of B-ingot.

bination centers to lower the MCLT. The other reason might be the high density of defects which were produced during the solidification and post solidification period. In this experiment, only one seed was employed at the bottom of the crucible. Normally, in the production of the mono-like mc-Si ingot, many seeds were placed at the bottom of the crucible. In that case, the gap between the seeds might act as a generation center of dislocation. Thus, a higher density of dislocation was observed normally at the top of the ingot. However, although there was no gap between the seeds, a high density of dislocation was present at the top position of the ingot as can be seen in Fig. 3. This observation indicates that the thermal stress developed near the top position of the ingot was high enough to generate the dislocation. Thus, to improve the quality of the silicon ingot, the reduction of the thermal stress is necessary. In the crystal growth process, reduction of the thermal stress can be fulfilled through slower solidification and cooling.

As can be seen in Fig. 3, optical photographs show the defect pattern of each silicon sample. It was observed that MCLT was inversely proportion to the defects density. After etching, it was found that the areas where high densities of defects present were revealed as whiter area in the photograph. In this area, the MCLT was lower than the other area. Lower MCLT was specifically taken at the grain boundary where a high density of dislocation was agglomerated. The average MCLT values taken at each position of the two ingots were shown in Fig. 4. As can be seen in the figure, MCLT values of the B-ingot were higher than the A-ingot regardless of the position. This observation is another indication that higher cooling of the ingot will give rise to thermal

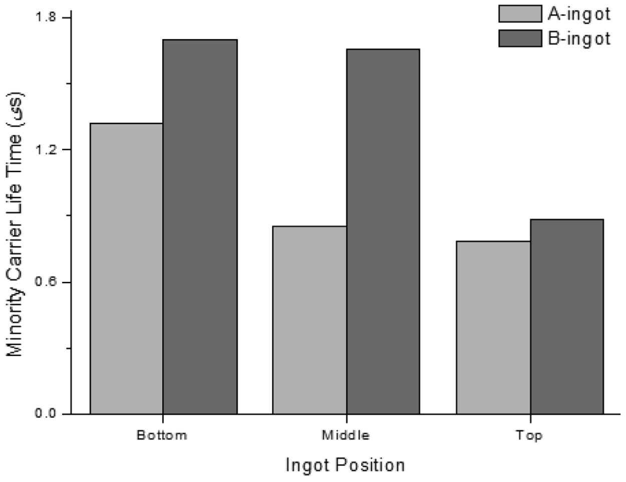

Fig. 4. The MCLT value from each position of two ingots.

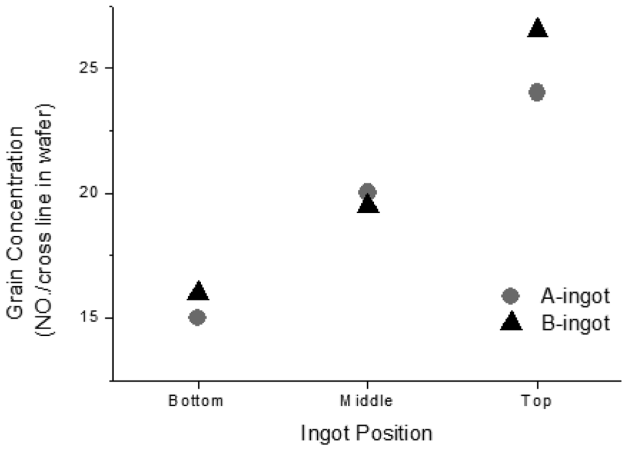

Fig. 5. Number of grain boundary crossing the line in wafer.

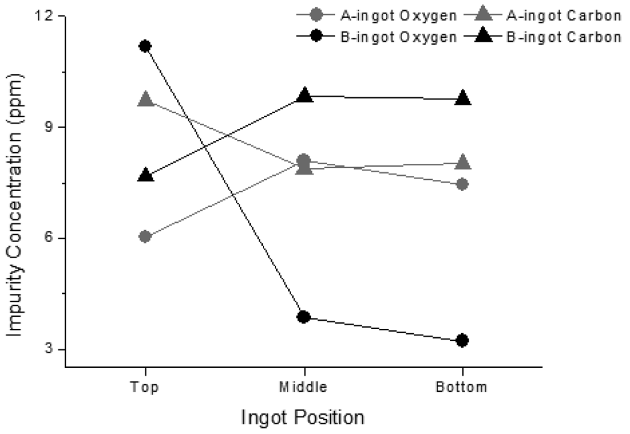

Fig. 6. Concentration of oxygen and carbon in each position of two ingots.

stress and, in turn, decrease to the MCLT value.

The effect of grain size on the MCLT value for these two silicon ingots is shown in Fig. 5. Although there is reliable difference in the MCLT observed between these two silicon ingots, there is no clear difference in grain size observed as shown Fig. 5. This observation might indicate the possibility that grain boundary itself will not lower the MCLT but some defects like dislocation will be responsible for lowering MCLT. Dislocations can be present at the grain boundary or within the grains. The grain boundary itself acts as barrier for electrical carriers. However, the dislocation agglomerated at the grain boundary might not add the carrier interruption effects to the crystal itself. However, if this defect is present within the grains, then it will affect the movement of the electrical carrier.

3.2. Relationship between MCLT and Impurities

To determine the other factors that might affect the MCLT, the concentration of O_i and C_s are measured with Fourier Transform Infrared Spectrometer (FT-IR) at each position of the two ingots as shown in Fig. 6. There is a clear difference in O_i between the two crystals. In A- ingot, O_i decreases with crystal growth from the bottom to the top. However, O_i increases in B-ingot from the bottom to the top of the ingot. This difference might be due to the different thermal history of the two ingots. Since crystal growth parameters are different for these two ingots, there must be a difference in the oxygen precipitation behavior. This possibility will cause a difference in O_i values as can be seen in Fig. 6. Since the crucible of this experiment is coated with silicon nitride, the total concentration of the oxygen contained in the silicon ingot is far below super saturation. Thus oxygen precipitation and related defect generation will be much less than in CZ-grown silicon crystal. It is well-known that oxygen and carbon atoms help each other to make precipitation in CZ silicon crystal. However, as can be seen in Fig. 6, there is no general relationship observed between oxygen and carbon atoms in this experiment.

3.3. Relationship between MCLT and Defects

It is well-known that crystal defects will affect the MCLT of the silicon crystal. In this experiment, twin boundary is observed to be present in the silicon crystal. Thus, it would be interesting to see the relationship with density of twin boundary and MCLT. First, density of twin boundary is measured at the silicon specimen of each position as shown in Fig. 7 and 8. Density of twin boundary is measured by the number of twin boundary crossing the line under the microscope. As can be seen in Fig. 7, density of twin boundary is the highest at the bottom position of the two ingots. This observation

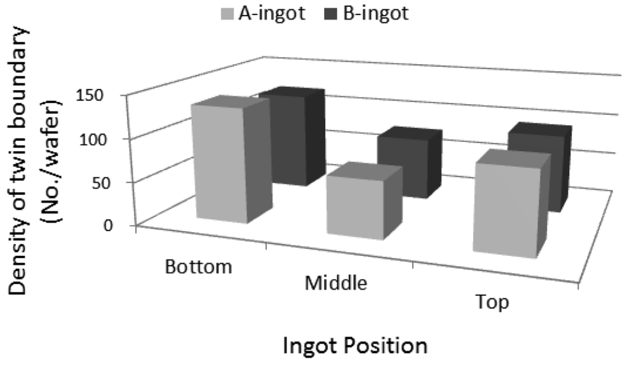

Fig. 7. Density of twin boundary in each position of the two ingots.

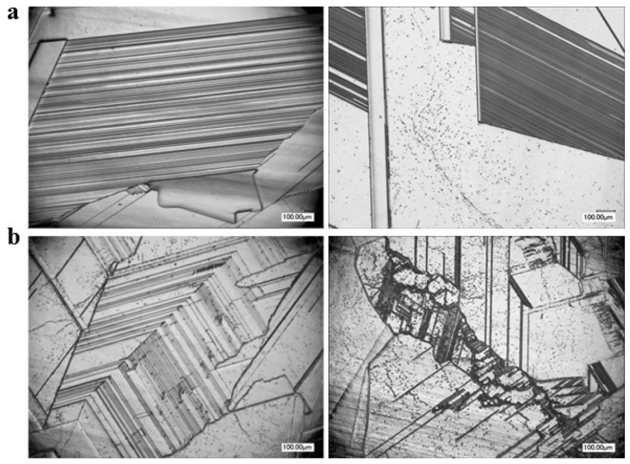

Fig. 8. Photograph of defects observed by optical microscopy (×100): (a) twin boundary at the high MCLT area, (b) twin boundary at the low MCLT area.

doesn't have any relationship with MCLT in Fig. 4. This might indicate the possibility that the twin boundary is not the defects deteriorating the MCLT in the silicon crystal. The shape observed with optical microscope is shown in Fig. 8. Interestingly, twin boundary itself will act as barrier for the twin boundary propagation. Also, there are two kinds of area where twin boundary and dislocation are present together. In one area like in Fig. 8a, very low density of dislocation etch pits (DEP) is found to be present near the twin boundary and some of the dislocation etch pits are present along the twin boundary. In this area, the MCLT is significantly high. In the other area, like in Fig. 8b, high density of DEP is observed to be present near the twin boundary. It was found that the MCLT is low in this area. Thus, there might be a time discrepancy in the generation of those two defects during the growth of the silicon crystal. It seems that if the twin boundary is formed first, dislocations will be formed along the twin plane later upon the thermal stress. This phenomenon will result in the defect configuration as in Fig. 8a and the resulting MCLT is higher. However, if the dislocations are formed first, the twin boundary is formed later irrespective of dislocation present. In this case, dislocations are present near the twin boundary as shown in Fig. 8b. This configuration will result in a lower value of MCLT.

It would be interesting to compare the MCLT of the two areas where dislocation density is highest and lowest. This observation is shown in Fig. 9 and 10. As can be seen in this figure, dislocation density is inversely proportion to the MCLT. Furthermore, in this silicon crystal, a high density of dislocation accompanies the high density of grain boundary. In this case, it might be expected that high stress is produced in this area first for various reasons, and consequently a high density of dislocation will be formed. Further, this high density of dislocation will be agglomerated to form grain boundary.

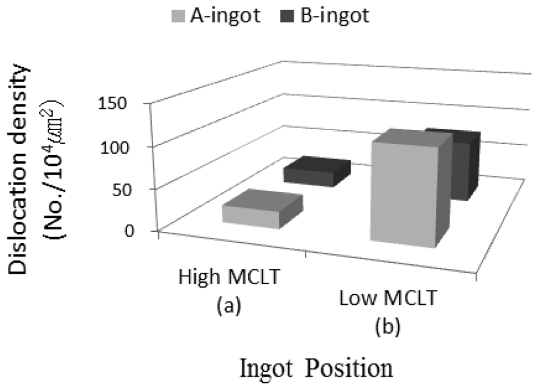

Fig. 9. The dislocation density at the high and low MCLT area.

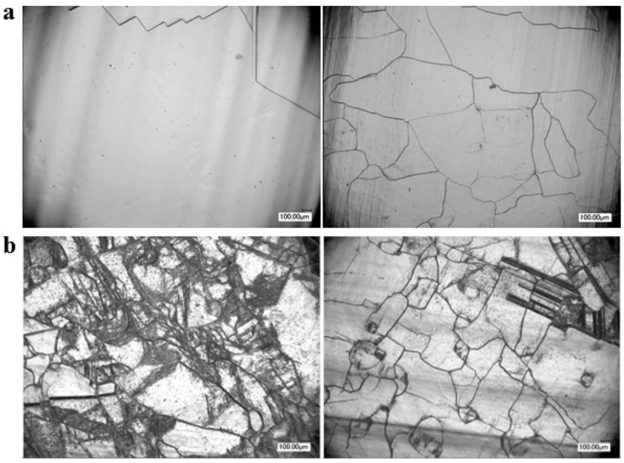

Fig. 10. Photograph of dislocation density in the specimen (×100): (a) at the high MCLT area, (b) at the low MCLT area.

3.4. Relationship between MCLT and Residual Stress

It would be interesting to see the effect of residual stress on the MCLT of the silicon crystal. As can be seen in Fig. 3, very low MCLT was measured at the edge of silicon crystal. In this mc-Si, this might be due to the dislocation developed along the wall of the crucible. However, it is well-known that a significantly low value of MCLT was measured at the edge of the CZ-silicon crystal, where not even one dislocation is present. Thus, it would be reasonable to expect that residual stress will affect the MCLT in mc-Si crystal.

A relative amount of residual stress in the silicon crystal can be compared by measuring the TTV, warp, bow, and saw mark of wafers after the slicing of ingot.

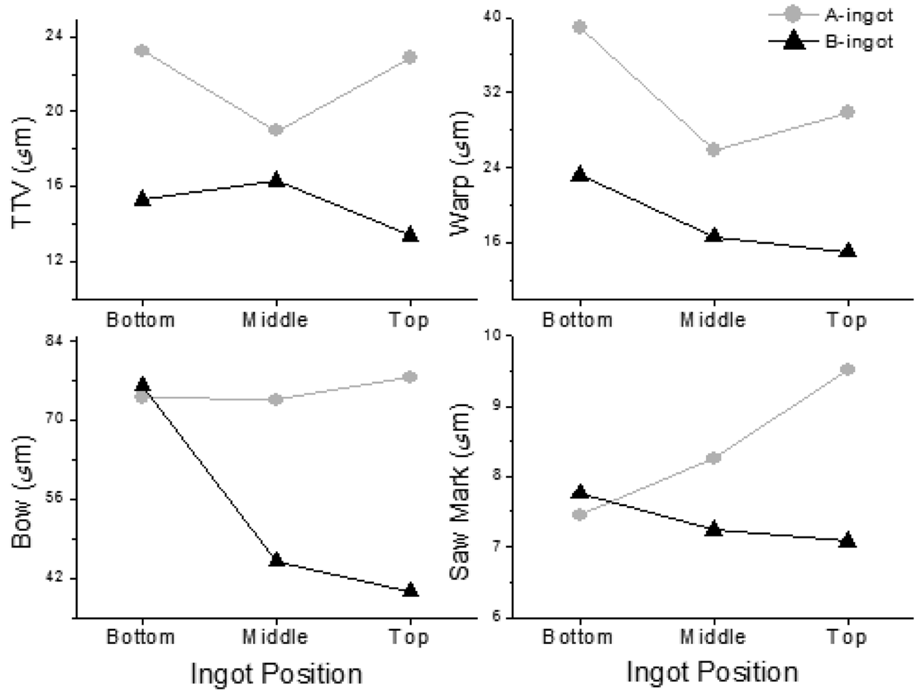

Fig. 11. The measurement of TTV, warp, bow, saw mark in each position of the two ingots.

It is expected that the ingot grown with a lower speed of solidification and cooling will have a lower amount of residual stress and the resulting silicon wafers will have a lower value of TTV, warp, bow, and saw mark. In Fig. 11, the measured value of TTV, warp, bow and saw mark of the silicon wafers taken from the two ingots. As can be seen in this figure, for most cases, B-ingot has a lower value of TTV, warp, bow and saw mark than A-ingot. This might be due to the longer time of cooling after the solidification is complete. In this experiment, it was found that the cooling process after solidification will be one of the critical processes governing the residual stress and relating the MCLT of the mc-Si solidified with directional solidification technique.

4. Conclusions

1) During the growth process of the mc-Si with directional solidification process, various defects such as dislocation, grain boundary, and twin boundary are formed. Also, residual stress remains in the mc-Si and the relative amount of this stress can be confirmed with the measurement of TTV and bow after the slicing of the silicon ingot.

2) Dislocation will be the major defect affecting the MCLT mc-Si grown with directional solidification process. Thus, the upper part of the mc-Si ingot gives the lowest value of MCLT because of the fastest cooling among the various portions of the mc-Si ingot.

3) There is no clear relationship between the twin boundary or grain boundary and MCLT in mc-Si. This observation might indicate that these two defects are not formed during the cooling period of the mc-Si growth process.

4) There is a clear relationship between the TTV or bow of the silicon specimen and MCLT. This observation might indicate that residual stress might be another main factor affecting the MCLT of mc-Si grown with directional solidification.

5) Conclusively, it can be said that cooling rate control will be the key factor enhancing the MCLT of mc-Si grown with directional solidification.

Acknowledgement

This work was supported by the Incheon National University (International Cooperative) Research Grant in 2014.

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