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A CMOS LNA based on Inverter Structure for Wideband Applications

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ABSTRACT

In recent years, the potential technology for short distance and high-data wireless communication systems has been grown. Ultra-wideband (UWB) technology has emerged as a considerable interest and new technology. According to a proposed standard, the UWB system is assigned to operate over 3.1 - 5 GHz or 3.1 - 10.6 GHz. Most of the proposed applications allow transmission of signals between 3.1 and 10.6 GHz. In this paper, a wideband CMOS Low Noise Amplifier (LNA) is proposed with a inverter structure using inductor peaking technique and broadband matching techniques, which meets stringent requirements of UWB system in the proposed specifications. The proposed LNA has the inverter structure and cascode structure with shunt feedback. Measurement results show the maximum power gain (S21) of 17.4 dB with the 3-dB band and input/output reflection coefficient (S11, S22) of less than −9.7 dB from 3.1 to 9.6 GHz. In addition, the fabricated LNA achieves the minimum noise figure (NF) of 3.5 dB from the operating frequency, which value is much lower than previously reported state-of-the-art wideband amplifiers. The input-referred IIP_3 and the input-referred $P1dB$ of the proposed LNA are achieved as 0 dBm and −10 dBm, respectively, while consuming 27 mW in 0.18-μm RF CMOS process.

KEYWORDS: Ultra wideband, Low noise amplifiers, Inverters, Cascode, Inductor peaking

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1. Introduction

During last few years, a newly effective strategy for ultra wideband (UWB) wireless communication, and software defined radio (SDR) has become more attractive to applications for small range and high data rate system. Ultra wideband (UWB) has emerged as a optimum technology capable of transmitting data with low power consumption and high-speed wireless communications.

Commonly, this technology has several strengths such as a simplicity, low cost, low power, and high-speed data rate wireless connectivity system among devices within or entering the private operating space. UWB communication system are permitted at a very low average transmit power compared to more conventional communication systems that practically restricts UWB to short distances. UWB is, thus, a suitable system for IEEE 802.15 Wireless Personal Area Network (PAN) with short distance and high data rate connectivity technology that complements other wireless communication systems.

The Low Noise Amplifier (LNA) is one of the most critical active devices in front end of a wireless receiver system. LNA's goal is to amplify a very low-power signal without significantly degrading its signal to noise ratio. Its role makes a decision about the overall receiver system sensitivity. This is accomplished by building an suitable matching condition located between the antenna and the LNA. But the implementation of an LNA is full of trade-offs between noise figure, gain, input-output matching, linearity, and power consumption.

Recently, in designing a wideband amplifier, the inverter structure or common-source structure with RC feedback are most widely used. The inverter based amplifier is also extensively utilized in digital and analog amplifiers for low power and high gain system in the CMOS technology [1-5].

The restive feedback inverter structure has been lately considered as the best structure for wideband applications because of the strengths such as better stability and wider bandwidth. Feedback configuration was used in the proposed LNA because it is more appropriate for integration due to better stability and uniformity at frequencies below 10 GHz.

Among recently published CMOS LNAs, Amplifiers with various structures are introduced for wideband applications. As described in [1-5], a wideband amplifier is proposed with flat gain and acceptable input matching condition. Although, the amplifier using common gate structure has a better matching behaviour for wideband frequency range, it has a bad NF performance. The amplifier using common source structure has a low NF, but its input impedance matching is difficult.

In the proposed LNA, a LNA based on the inverter structure is used as a main amplifier. The inverter structure is selected because of its better input impedance matching and low noise for wideband applications. In addition, A cascode structure is used at the output stage for high gain and good output impedance matching. This paper

presents the Low Noise Amplifier for wideband applications, which utilizes the inverter structure with inductor peaking and cascode feedback structure using 0.18-μm RF CMOS technology.

In Section 2, the concept of UWB LNA requirement is carefully described. Section 3 presents the LNA structure and the design approach of the proposed LNA. The measured results are presented in Section 4. Finally, the conclusions are in Section 5.

2. Concept of Wideband LNA Requirement

In the system of mobile wireless communication, the first stage of a receiver system is commonly an LNA, whose main role is to offer enough gain to overcome the noise of subsequent active devices (such as mixer), but not so much to cause the mixer overload. Secondly, an LNA should include as little noise as possible to minimize the effect on the general noise performance. For wireless communication systems, the LNA noise figure (NF) needs to be lower than 3～4 dB because unavoidable losses of RF filter remain little noise budget for other active blocks. According to the multi-band OFDM for IEEE 802.15.3a, the overall NF for the RF CMOS front-end is approximately 6.9 dB. The overall NF which include losses with the pre-select filter and the duplexer is 8.6 dB [6]. If the NF of mixer is 12 dB, the power gain of LNA and the conversion gain of the mixer are 15 dB and 10 dB respectively, then the NF of LNA would not be less than 4 dB according to Friis equation [7]. Therefore, when the LNA's gain and NF is 15dB and less than 4 dB respectively, the receiver sensitivity requirement can be satisfied with UWB applications. Moreover, to avoid reflections on transmission line connecting the off-chip antenna to the on-chip LNA, an LNA must also present 50 Ω to the input source [8].

3. Circuit design

3.1 The structure based on inverter with peaking inductor for input matching

The proposed schematic for input matching is the structure based on inverter. Figure 1 show the conventional inverter gain structure without resistive-feedback(R_f), the conventional resistive-feedback inverter gain structure without peaking inductor(L_g), and with peaking inductor (L_g) [9, 10].

<Figure 1(a)> shows the inverter structure which uses PMOS and NMOS pairs. This technique can also achieve the same noise figure and input impedance with half of the power consumption required for a conventional NMOS device [3]. <Figure 1(b)> shows the conventional resistive-feedback inverter gain structure without inductive peaking.

The time constant at the input·output node can dominate the bandwidth of the conventional feedback inverter [2, 11]. Accordingly, the operating bandwidth will be deteriorated by the parasitic capacitors of the CMOS devices.

<Figure 1(c)> shows the proposed inverter with a inductive peaking technique at the gate of

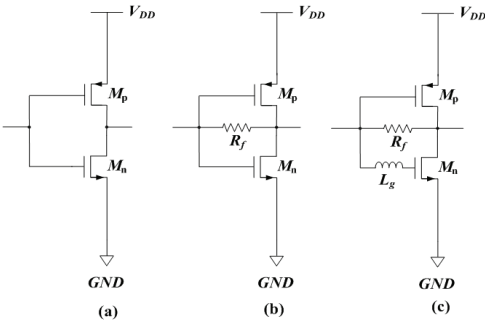

Figure 1. The structure based on inverter. (a) general inverter. (b) the conventional resistive-feedback inverter structure without inductive peaking. (c) the conventional resistive-feedback inverter gain structure with inductive peaking.

NMOS device. By applying inductive peaking technique asymmetrically at the gate of NMOS in the inverter, the capacitive loads from the PMOS and NMOS can be divided due to the exploitation of the peaking inductor. Thus, the 3-dB bandwidth can be further extended to a higher frequency [2]. The transfer function of <Figure 1(c)> can be derived as

$$\frac{V_{out}}{V_{in}} = \frac{1}{1+s^2 L_g C_{gsn}} \times \frac{1-R_f(g_{mp}+g_{mn})+s^2 C_{gsn} L_g (1-g_{mp}R_f)}{1+R_f(sC_{dsn}+sC_{dsp}+1/r_{on}+1/r_{op})} \quad (1)$$

where C_{gsn} is the gate-source capacitors from the gate of NMOS, g_{mp} and g_{mn} are the transconductance of the PMOS and NMOS, respectively. C_{dsn} and C_{dsp} are the capacitors between the drain and source terminals, and r_{op} and r_{on} are the output resistance of the PMOS and NMOS, respectively. From (1), it can be observed that the characteristic at higher frequencies is improved. To achieve a flat gain with wideband characteristic in the proposed structure, an inverter stage with splitting-load inductive peaking technique is utilized.

$$NF = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{G_1} + \cdots + \frac{NF_N - 1}{G_1 G_2 \cdots G_{N-1}} \quad (2)$$

The Noise Figure is dominated of the first stage for the multi-stage amplifier due to the total NF. where NF is the total noise figure and NF_N and G_N are the Noise Figure and power gain of N^{th} stage.

The first stage of the receiver system is the LNA. Therefore, lowering the Noise Figure is of critical importance for the LNA implementation. Based on equation (2), the gain of the first stage is high enough to moderate the influence of second stage in the total NF. In the proposed LNA, as can be seen, the feedback resistor R_f in the first stage is utilized to stabilize the gain and amplify the bandwidth of the inverter structure. The feedback resistor R_f is optimized for minimum NF across the operating bandwidth [10].

The measured minimum NF in the proposed LNA is 3.5 dB. The average NF in the operating frequency range achieves low value compared with that of previously designed wideband LNAs.

3.2 LNA Design for Wideband applications

<Figure 2> shows a proposed wideband CMOS LNA circuit schematic. The proposed wideband LNA is composed of two stages, designed with

Cadence SpectreRF based on TSMC 0.18-μm RF CMOS technology.

The first stage consists of a resistive-feedback (R_{f1}) inverter based structure with peaking inductor(L_g) and input matching network. Since the first stage's device seriously affect the noise characteristics of LNA and also the first stage entirely contributes to the total noise figure, the first stage's device size(M_1, M_2) and bias voltage should be optimized for the low NF. In the approach used, the device size is chosen to obtain the least NF at desired drain current.

To overcome the large input parasitic capacitance, the inductor(L_s) of the first stage are adopted for the partial tuning-out of the input parasitic capacitances [12]. The gate optimum bias voltage(V_{g1}) for the first stage [13] are finally designed for the low NF and bandwidth. The second stage consists of a cascode feedback structure. According to [14], the cascode structure has significant properties such as high gain, high reverse isolation, and broad bandwidth. In the LNA design procedure, the second stage of LNA should generally analyze the performance of linearity because the last stage is a important factor to determine the linearity [15]. For a cascaded amplifier, the total input-referred third-order intercept point($IIP_{3,total}$) is expressed as

$$\frac{1}{IIP_{3,}} \approx \frac{1}{IIP_{3,1}} + \frac{\alpha_1^2}{IIP_{3,2}} + \frac{\alpha_1^2\beta_1^2}{IIP_{3,3}} + \cdots\cdots \quad (3)$$

where α_1 and β_1 are the linear gains for the first and second stages, respectively. Equation (3) shows that the last stage's IIP_3 significantly affects the total IIP_3. Thus, the transistor size and bias voltage of the second stage are designed for the linearity improvement and high gain with restricted power consumption. The gate width of M_3 is chosen for high gain. The gate bias voltage(V_{g2}) is chosen for M_3.

In order to yield a flatter and broader bandwidth, tank circuits of L_{load} and C_d are also designed. R_d and C_d by pass networks are added

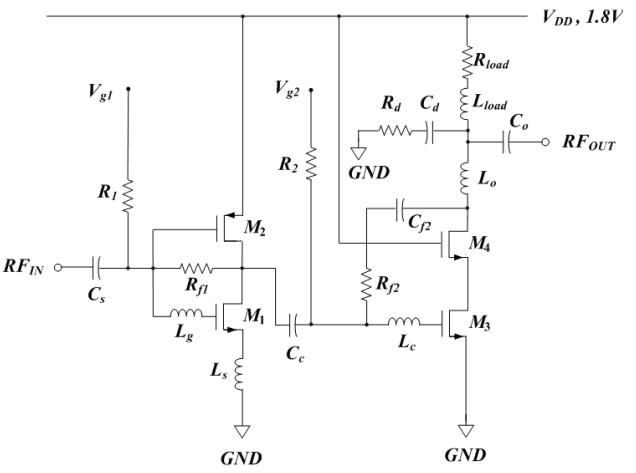

Figure 2. Circuit schematic of the proposed wideband CMOS LNA

with dc bias paths to assure a better gain and stability for a low frequency. It also affects the wideband output matching. L_c of the second stage can improve the power gain and noise figure of LNA at a high frequency. L_o can provide the function of the inductive peaking and work as the loads of device M_1.

4. Measurement results

The post-layout circuit simulation of the LNA has been performed with Cadence SpectreRF based on TSMC 0.18-μm RF CMOS technology. When 1.8 volts is supplied, a total current of the proposed amplifier has only 15 mA. Due to a high sheet resistance of the poly gate of RF MOSFET, a multi-finger layout technique is used to improve its RF performance and to lower the noise of the RF MOSFET's gate resistance. It has also been considered for reducing the parasitic capacitance and resistance on RF signal. The chip photo is shown in <Figure 3>. The die area including testing pads is only 1.15 × 0.95 mm^2

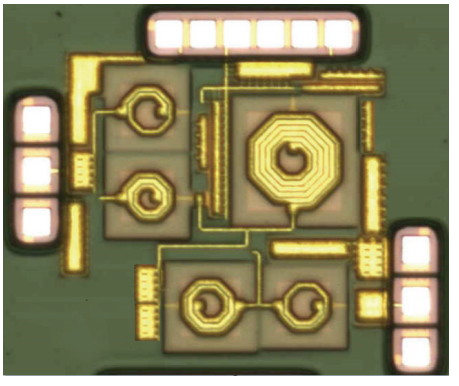

Figure 3. Chip photo of the designed LNA

The size of on-chip spiral inductor mainly determine the chip size. <Figure 4> shows the simulated spiral inductor characteristics for inductor (L_g) of the input stage. The characteristics of quality factor for the designed inductor was basically analyzed using TSMC 0.18-μm RF CMOS technology. As shown in <Figure 4>, W is the inductor track width and R is the inner radius of inductor. In order to improve better LNA performance in the operating frequency band, an inductor of good quality factor is required. To obtain the desired inductor with a good quality factor for operating frequency bands, the design parameters for inductor were obtained through the simulation.

As shown in <Figure 5>, the fabricated LNA achieves a maximum power gain(S_{21}) of 17.4 dB at 3.7 GHz with parasitic effects. The flatness of gain within 3 dB in the frequency range of operation indicates suitability for UWB applications.

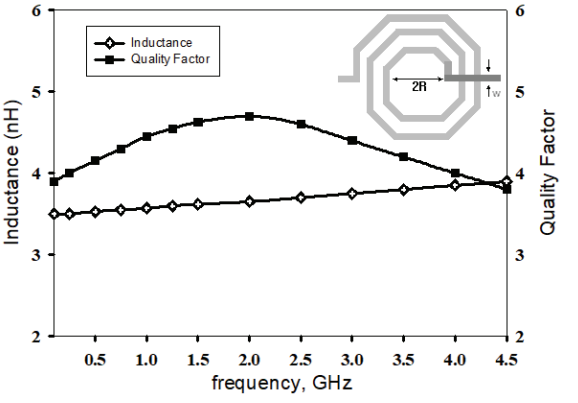

Figure 4. Simulated spiral inductor (L_g) characteristics; Inductances and quality factors with top view of a spiral inductor layout

The input return loss(S_{11}) and output return loss(S_{22}) measurement results are shown in <Figure 6>. The measured S_{11} of less than −10 dB and S_{22} of less than −9.7 dB are obtained over 3.1 ~ 9.6 GHz.

This proves the effectiveness of the broadband input·output matching realized by the resistive feedback inverter based structure with inductive peaking and the structure of the output matching used by LC tank.

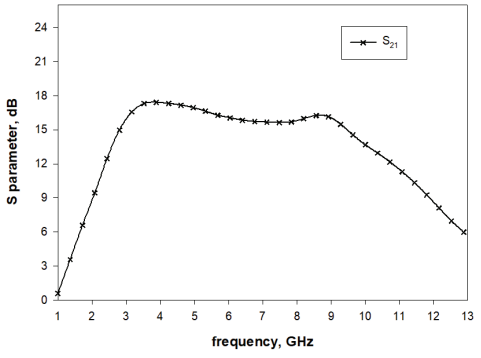

Figure 5. The measured power gain(S_{21})

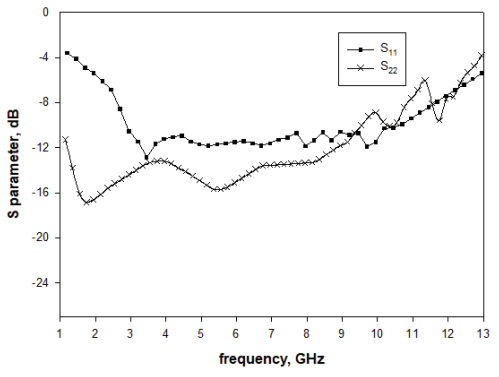

Figure 6. The measured input return loss(S_{11}) and output return loss(S_{22})

The measured noise figure of LNA is plotted in <Figure 7>. The maximum NF at 9.6 GHz is 4.3 dB. In the frequency range of interest (3.1 ~ 9.6 GHz), the NF is between 3.5 dB and 4.3 dB. This low value is attributed to the noise impedance matching.

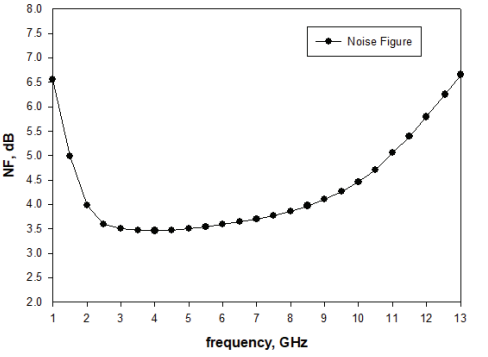

Figure 7. The measured Noise Figure

The measurement result in <Figure 8> indicates a 0 dBm input referred third-order intercept point (IIP_3). In addition, <Figure 8> shows a input 1 dB compression point($P1dB$) of −10 dBm. These results demonstrated that good linearity and high dynamic ranges of the LNA were implemented. The total power consumption of the proposed LNA is 27 mW.

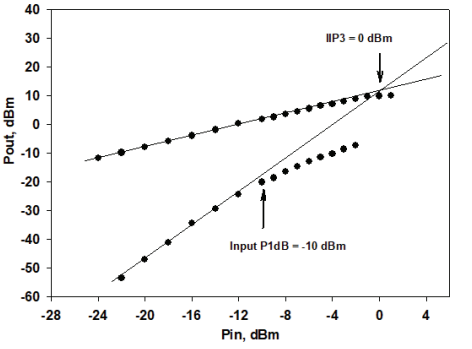

Figure 8. The measured IIP_3 and $P1dB$

Table 1. Performance summary and comparison to with other UWB CMOS LNAs.

Ref.	Bandwidth (GHz)	NF_{min} (dB)	$S_{21\ max}$ (dB)	S_{11} (dB)	IIP_3 (dBm)	Power(mW)	Tech.
[1]	3.1～10.6	4.5	14	< -11	-12	21	measured $0.18\mu m$
[5]	1～11	2.5	17	< -10	-7.5	11.3	measured $65\ nm$
[16]	3.1～10.6	4.5	13.2	< -9.5	-1.4	23	measured $0.18\mu m$
[17]	3.1～10.6	3.1	16	< -8.0	-7	11.9	measured $0.18\mu m$
[18]	3.1～10.6	3.7	12.8	< -8.6	-11	10.34	measured $0.18\mu m$
This work	3.1～9.6	3.5	17.4	< -10	0	27	measured $0.18\mu m$

The performance summary of the proposed LNA is listed in <Table 1> and compared with those of previously designed 0.18-μm CMOS LNAs.

The performance of power gain (S_{21}) in the proposed LNA are better than the LNA reported in <Table 1>. The proposed LNA attains good NF compared with other wideband LNAs. In addition, it can be seen that the measured S_{11} of the proposed LNA has good 10 dB return loss bandwidth, but S_{22} does not satisfy sufficient 10 dB return loss bandwidth in high band.

As can be seen, The value of power gain(S_{21}) and input return loss(S_{11}) with the designed LNA is better than found in other papers.

5. Conclusions

In this paper, an UWB LNA that uses the resistive feedback inverter based structure with peaking inductor and cascode structure was presented. The proposed LNA consists of two stages, whereby wideband with low noise, high gain and linearity are separated into each stage. This wideband amplifier were designed in 0.18-μm RF CMOS technology to demonstrate the proposed techniques for bandwidth enhancement. Using the resistive feedback inverter structure with inductive peaking is extended to 9.6 GHz. Also better input matching is achieved with lower noise and high gain.

This amplifier has less than 4.3 dB noise figure, 17.4 dB maximum power gain, and less than −10 dB input return loss from 3.1 GHz to 9.6 GHz. This measurement results shows a good performance for wideband LNA. Therefore, the designed wideband LNA can be used for UWB applications.

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광대역 응용에 적합한 인버터 구조의 CMOS 저잡음 증폭기

정지학

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요 약

최근에는, 짧은 거리와 대용량 데이터 무선 통신 시스템에 대한 잠재적인 기술들이 지속적으로 성장해 왔다. 그리고 초광대역 기술은 상당한 관심과 새로운 기술로서 부각되어왔다. 제안된 표준에 따르면, UWB 시스템은 3.1 ~ 5 GHz 또는 3.1 ~ 10.6 GHz 에 대해서 동작하도록 할당 된다. 대부분의 제안된 응용분야에서는 3.1 ~ 10.6 GHz 사이의 신호 전달을 할당한다. 본 논문의 광대역 저잡음 증폭기는 인덕터 피킹 기법을 이용한 인버터 구조와 광대역 정합 기술을 제안하였는데, 이러한 기술은 제안된 사양의 까다로운 UWB 시스템 요구사항을 만족한다. 제안된 저잡음 증폭기는 인버터 구조 및 shunt 저항을 사용한 캐스코드 구조로 이루어져 있다. 측정 결과는 3.1 ~ 9.6 GHz 대역 내에서 최대 전력 이득은 17.4 dB, 입력 정합은 -10 dB 이하, 출력 정합은 -9.7 dB 이하 이며 최소 잡음지수는 3.5 dB를 보여준다. 최소 잡음지수 값은 이전에 기록된 최근의 광대역 증폭기들 보다 낮은 값이다. 제안된 증폭기의 입력 IIP_3 는 0 dBm, 입력 $P1dB$ 는 -10 dBm 이며, 전체 소비전력은 27 mW 를 가진다.

Ji-Hak Jung received the Ph.D. degree in the Department of Electronic Communication and Radio Engineering from Hanyang University in 2006. From 2006 to 2015, he was a Principal engineer at SAMSUNG Electronics S-LSI. He has been a professor in the Department of Semiconductor & Display at Asan Campus of Korea Polytechnics since 2016. His current research interests include intelligence semiconductor, RF system, RF IC, active device, and mobile communication system.

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